CLAIMS

1. A reconfigurable processing system, which allows for the implementation of a variety of system configurations with minor hardware and software modifications, said system comprising:

a primary processing system including a primary peripheral bus, said primary peripheral bus having a predetermined bus structure;

at least one secondary processing system including a secondary peripheral bus, said secondary peripheral bus having the same predetermined bus structure as said primary peripheral bus; and

and a peripheral bus coupler, wherein said secondary peripheral bus serves as a local bus to said secondary processing system and interfaces at least one secondary processing system component with said primary processing system via said peripheral bus coupler and said primary peripheral bus.

2. The reconfigurable processing system as claimed in claim 1, wherein said peripheral bus coupler comprises a peripheral bus bridge.

3. The reconfigurable processing system as claimed in claim 1, wherein said peripheral bus coupler comprises a network interface.

4. The reconfigurable processing system as claimed in claim 1, wherein said predetermined bus structure comprises a Peripheral Component Interface (PCI) bus structure.

5. The reconfigurable processing system as claimed in claim 1, wherein said at least one secondary processing system component comprises an accelerator subsystem, including a processing accelerator.

6. The reconfigurable processing system as claimed in claim 5, wherein said accelerator subsystem further comprises at least one image memory interfaced with said processing accelerator via an image memory data bus.

7. The reconfigurable processing system as claimed in claim 4, wherein at least one secondary processing system component comprises a digitizer subsystem.

8. The reconfigurable processing system as claimed in claim 7, wherein said secondary processing system comprises a PCI bus add-in extension board and said digitizer subsystem comprises

a digitizer daughter card attached and electrically connected to said PCI add-in extension board using a PCI bus compatible connector.

9. The reconfigurable processing system as claimed in claim 8, wherein said digitizer daughter card comprises a camera interface, a master direct memory access (DMA) controller and field input/output (I/O) controllers, which receive and organize a stream of related data samples, route said organized data samples to memory locations and control input and output ports to support system operations and facilitate intercommunications with other devices.

10. The reconfigurable processing system as claimed in claim 8 further comprising a vision CPU subsystem including a vision system CPU, a host bus bridge for interfacing said vision system CPU with said host CPU peripheral bus and said vision processing system peripheral bus, at least one system peripheral, local system memory, and a local display controller, including local display memory.

11. The reconfigurable processing system as claimed in claim 1, wherein said secondary processing system includes a vision processing system, said vision processing system comprising:

a vision accelerator subsystem including a processing accelerator and at least one image memory interfaced with said processing accelerator via an image memory data bus;

a digitizer subsystem including a digitizer, a direct memory access (DMA) controller, a field input/output (I/O) controller and at least one camera; and

a vision central processing unit (CPU) subsystem including an embedded vision system CPU, a host bus bridge for interfacing said vision system CPU with said secondary peripheral bus, system memory, at least one system peripheral, a display controller including display memory for interfacing a local display to said secondary peripheral bus.

12. The reconfigurable vision processing system as claimed in claim 4, wherein said at least one vision processing system component includes an identification selection (IDSEL) signal line, which is variably connectable and disconnectable to said a PCI address and data line in the range AD [15:11] on said vision processing system PCI bus to hide said at least one vision processing system component from said host CPU PCI bus.

13. A reconfigurable vision processing system comprising:

a host central processing unit (CPU) having a Peripheral Component Interface (PCI) peripheral bus, said host CPU including host memory and a digitizer subsystem including a digitizer, a direct memory access (DMA) controller and a field input/output (I/O) controller for receiving and organizing a stream of related data samples, routing said organized data samples to said host memory and controlling input and output ports to support vision system operation and facilitating intercommunications with other devices, respectively.

14. In a reconfigurable processing system wherein a host central processing unit (CPU) interfaces primary peripheral components via a primary, host Peripheral Component Interface (PCI) bus and secondary processing system peripheral components via a secondary processing system PCI bus over a PCI to PCI bus bridge, a method of hiding a processing system peripheral component from said host peripheral bus comprising the step of connecting said peripheral device's identification selection (IDSEL) line to said secondary, vision processing system PCI bus at PCI address and data lines in the range AD[15:11].

15. In a reconfigurable vision processing system wherein a host central processing unit (CPU) interfaces primary peripheral components via a primary, host Peripheral Component Interface (PCI) bus and secondary, vision processing system peripheral components via a secondary, vision processing PCI bus over a PCI to PCI bus bridge, an apparatus for disconnecting and hiding a secondary, vision processing system peripheral component from said primary, host PCI bus comprising:

a state machine used to control said vision processing system peripheral component's reset release and identification selection (IDSEL) connection sequencing by disconnecting said peripheral component from said secondary, vision processing PCI bus until it is ready to accept bus transactions.

16. In a reconfigurable vision processing system including a host central processing unit (CPU) interfacing primary peripheral components via a primary, host Peripheral Component Interface (PCI) bus and secondary, vision processing system peripheral components via a secondary, vision processing system PCI bus over a PCI to PCI bus bridge, said vision processing system further including a vision processing subsystem having an embedded CPU, said embedded CPU interfacing said primary and secondary peripheral busses via a host bus bridge, a method of resetting said embedded CPU comprising:

creating a back-door signal from said PCI to PCI bus bridge and attaching said back door signal to said secondary, vision processing PCI bus' general purpose input/output (GPIO) port.

17. In a reconfigurable vision processing system including a host central processing unit (CPU) interfacing primary peripheral components via a host Peripheral Component Interface (PCI) bus and secondary, vision processing system peripheral components via a vision processing PCI bus over a PCI to PCI bus bridge, said reconfigurable vision processing system further including a vision processing subsystem having an embedded CPU, said embedded CPU interfacing said primary and secondary PCI busses via a host bus bridge, a method of testing and booting said embedded CPU comprising the step of: loading software code over said primary and secondary PCI busses from a source independent of said vision processing subsystem.

18. The method of claim 17, wherein said source of code is said host CPU.

19. The method of claim 17, wherein said source of code is an Ethernet device.

20. A processing system with memory reservation device, said system comprising:

a primary processing system including:

a primary peripheral bus, said primary peripheral bus having a predetermined bus structure; and

a Basic Input/Output operating System (BIOS), for at least allocating system memory to recognized devices interfaced to said primary peripheral bus in response to reading and recognizing a device class code stored in each said recognized device interfaced to said primary peripheral bus;

at least one secondary processing system including:

a secondary peripheral bus, said secondary peripheral bus having the same predetermined bus structure as said primary peripheral bus and serving as a local bus to said secondary processing system, and for interfacing at least one secondary processing system peripheral device with said primary processing system via a peripheral bus coupler and said primary peripheral bus; and

a surrogate peripheral device, said surrogate peripheral device having no significant peripheral device functionality and including a class code register containing a peripheral bus class code of a standard peripheral device; and

a peripheral bus coupler, coupled to said primary processing system and to said at least one secondary processing system, said peripheral bus coupler including said system allocatable memory to be allocated by said BIOS.

21. The system of claim 20 wherein said peripheral bus class code of a standard peripheral device includes an Ethernet device class code.

22. The system of claim 20 wherein said primary and secondary peripheral buses include PCI buses.